IN THE CLAIMS

We claim:

1. A process comprising:

providing a semiconductor substrate; and

coupling said semiconductor substrate directly to a bulk heat dissipation substrate having a thermal conductivity greater than that of said semiconductor substrate.

2. The process of claim 1 wherein said bulk heat dissipation substrate is silicon carbide.

3. The process of claim 1 wherein said bulk heat dissipation substrate is a material that removes heat from the semiconductor substrate.

4. The process of claim 1 wherein said coupling comprises:

forming a splitting layer within the semiconductor substrate;

bonding said semiconductor substrate chemically to said bulk heat dissipation substrate; and

splitting said semiconductor substrate along said splitting layer.

5. The process of claim 4 wherein forming said splitting layer comprises implanting said semiconductor substrate with a rare gas to form a rare gas implant layer.

6. The process of claim 5 wherein said rare gas is hydrogen.

7. The process of claim 1 wherein said coupling comprises:

bonding said semiconductor substrate chemically to said bulk heat dissipation substrate; and

grinding back said semiconductor substrate.

8. The process of claim 1 wherein said coupling comprises:

depositing said bulk heat dissipation substrate directly on said semiconductor substrate.

9. The process of claim 8 wherein said depositing of said bulk heat dissipation substrate comprises chemical vapor deposition.

10. The process of claim 1 further comprising forming a transition layer on said bulk heat dissipation substrate prior to said coupling.

11. The process of claim 10 wherein said transition layer is silicon nitride.

12. The process of claim 10 wherein said transition layer is polysilicon.

13. The process of claim 12 further comprising bonding said polysilicon transition layer to said semiconductor substrate.

14. The process of claim 13 wherein bonding said polysilicon transition layer to said semiconductor substrate comprises:

forming weak bonds between said polysilicon layer and said silicon layer; and

heating said polysilicon layer and said silicon layer to create covalent bonds between said polysilicon layer and said silicon layer.

15. A process comprising:

providing a silicon wafer;

implanting said silicon wafer with hydrogen to form a hydrogen implant layer within said silicon wafer;

depositing a silicon carbide layer on said silicon wafer by chemical vapor deposition;

splitting said silicon wafer along said implant layer to form a silicon layer on which said silicon carbide layer is deposited;

polishing said silicon layer; and

polishing said silicon carbide layer.

16. The process of claim 15 further comprising depositing said silicon carbide layer to a thickness in the approximate range of 0.5mm-1.0mm.

17. The process of claim 15 further comprising polishing said silicon carbide layer to a thickness in the approximate range of 750-800μm.

18. A substrate comprising:

a semiconductor wafer; and

a bulk heat dissipation wafer in contact with said semiconductor wafer and having a higher thermal conductivity than said semiconductor wafer.

19. The substrate of claim 18 wherein said semiconductor wafer comprises silicon.

20. The substrate of claim 18 wherein said bulk heat dissipation wafer comprises silicon carbide formed by chemical vapor deposition.

21. The substrate of claim 18 wherein said semiconductor wafer is covalently bonded to said bulk heat dissipation wafer.

22. The substrate of claim 18 wherein the elastic modulus of said bulk heat dissipation wafer is greater than the elastic modulus of said semiconductor wafer.

23. The substrate of claim 18 wherein the thermal expansion coefficient of said semiconductor wafer is approximately equal to the thermal expansion coefficient of said bulk heat dissipation wafer.

24. The substrate of claim 18 further comprising a transition layer between said semiconductor wafer and said bulk heat dissipation wafer.

25. A heat dissipation device comprising:

a silicon carbide wafer having a thickness greater than 100 μm;

a transition layer comprising polysilicon coated on said silicon carbide wafer, wherein said transition layer is planarized on a first side; and

a silicon wafer covalently bound to said first side of said transition layer.

26. The device of claim 25 wherein said silicon wafer has a thickness of between 750μm and 800 μm.

27. The device of claim 25 wherein said silicon carbide wafer has a thickness of between 750μm and 800 μm.

28. A microelectronic package comprising:

a die comprising a silicon substrate having a first surface having devices formed thereon and a second surface chemically bonded to a bulk silicon carbide substrate; and

a heat sink.

29. The system of claim 28 further comprising a first thermal interface material between said silicon carbide and said heat sink.

30. The system of claim 28 wherein said die further comprises a transition layer between said silicon layer and said silicon carbide layer.